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To: Examiner Annette Thompson

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From: Sara Chang

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Business Phone: (310) 785-0140

Home Phone:

Pages: 9

Date/Time: 12/10/2004 2:31:23 PM

Subject: Unsigned references on 1449 for 10061459

To Examiner Annette Thompson,

Thank you very much for your response to the fax I sent yesterday. I received your message that this may be a duplicate of something you've already signed and sent to us. However, there are no records showing signed IDS's of the ones I faxed to you on Thursday. If possible, please review it, sign it, and return to us.

Thank you again,

Sara Chang
Legal Assistant
310-785-0140 ext. 306

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DATE: December 8, 2004
TO: Examiner Annette Thompson
COMPANY: USPTO
FROM: Sara Chang
PAGES: 8 (including this page)

Examiner Annette Thompson:

For the application S/N 10/061,459, we received a Notice of Allowance mailed on 11/19/2004. Thank you for this Notice of Allowance. However, we noticed that your initials are not next to the references on the 1449 Form: of 3 IDS submitted on 10/20/2003, 12/1/2003, and 4/6/2004. We are including the 1449 Forms along with the return receipt postcard for your review in this fax. If possible, please initial the 1449 forms to indicate that you have considered them. If you have any questions, please give me a call.

Regards,

Sara Chang

Stattler, Johansen & Adeli LLP
1875 Century Park East
Suite 1050 10th floor
Century City, CA 90067-2501

Phone No. (310) 785-0140 Ext.300
Fax No. (310) 785-9558

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Substitute for form 1449A/PTO				Application Number	10/061,459
				Filing Date	1/31/02
				First Named Inventor	Steven Telg, et al.
				Group Art Unit	2825
				Examiner Name	Thompson, Annette
Sheet	1	of	2	Attorney Docket Number	SPLX.P0091

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document Number	Kind Code ² (If Known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
1.	2002/0157 063	A1		10-24-2002	Besson	
2.	2002/0178 432	A1		11-28-2002	Kim et al.	
3.	2003/0145 288	A1		07-31-2003	Wang et al.	
4.	4,703,435			10-27-1987	Darringer et al.	
5.	5,003,487			03-26-1991	Drumm et al.	
6.	5,537,330			07-16-1996	Damiano et al.	
7.	5,892,678			04-06-1999	Tokunoh et al.	
8.	5,903,466			05-11-1999	Beausang et al.	
9.	5,991,524			11-23-1999	Belkhale et al.	
10.	6,035,107			03-07-2000	Kuehlman et al.	
11.	6,080,204			06-27-2000	Mendel	
12.	6,218,252	B1		04-10-2001	Dangelo et al.	
13.	6,311,317	B1		10-30-2001	Khoche et al.	
14.	6,389,586	B1		05-14-2002	McElvain	
15.	6,397,170	B1		05-28-2002	Dean et al.	
16.	6,421,818	B1		07-16-2002	Dupenloup et al.	
17.	6,446,240	B1		09-03-2002	Iyer et al.	
18.	6,453,447	B1		09-17-2002	Gardner et al.	
19.	6,470,478	B1		10-22-2002	Borgh et al.	
20.	6,470,486	B1		10-22-2002	Knapp	

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Substitute for form 1449A/PTO				Application Number:	10/061,459.
				Filing Date:	1/31/02
				First Named Inventor:	Steven Teig, et al.
				Group Art Unit:	2825
				Examiner Name:	Thompson, Annette
Sheet	2	of	2	Attorney Docket Number	SPLX.P0091

U.S. PATENT DOCUMENTS					
21.	6,519,609	B1	02-11-2003	Touzet	
22.	6,519,754	B1	02-11-2003	McElvain et al.	
23.	6,539,536	B1	03-25-2003	Singh et al.	
24.	6,543,037	B1	04-01-2003	Limqueco et al.	
25.	6,546,541	B1	04-08-2003	Petranovic et al.	
26.	6,618,835	B1	09-09-2003	Garlapalli et al.	

NON-PATENT LITERATURE DOCUMENTS					
Examiner Initials:	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate); title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.			F ²
	27.	NN78055443, "Automatic Remap", IBM Technical Disclosure Bulletin, Vol. 20, No. 12, May 1978, pp. 5443-5445 (5 pages).			
	28.	NN9411291, "Design of Portable Library using Parameterized Cells", IBM Technical Disclosure Bulletin, Vol. 37, No. 11, pp. 291-292 (4 pages).			
	29.	Markovic et al., "FPGA to ASIC Conversion Design Methodology with the Support for Fast Retargetting to Different CMOS Implementation Technologies", Proceedings of 2002 22 nd International Conference on Microelectronics, Vol. 2, 14 May 2000, pp. 703-706.			
	30.	Ruiz et al., "Design and Prototyping of DSP Custom Circuits Based on a Library of Arithmetic Components", Vol. 1, 9 November 1997, pp. 191-196.			
	31.	Tamiya, Y., "Delay Estimation for Technology Independent Synthesis", 1997 Proceedings of the ASP-DAC '97, Asia and South Pacific Design Automation Conference, 28 January 1997, pp. 31-36.			
	32.	Yi, J. H. et al., Technology Mapping for Storage Elements Based on BDD matching, Proceedings of the 40 th Midwest Symposium on Circuits and Systems, pp. 1099-1102, vol. 2, August 1997.			

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Examiner Initials	Cite No. ¹	U.S. Patent Document Number ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
1.	5,519,630		05-21-1996	Nishiyama et al.	
2.	5,537,341		07-16-1996	Rose et al.	
3.	5,696,974		12-09-1997	Agrawal et al.	
4.	5,574,441		05-19-1998	Tokunoh et al.	
5.	5,787,010		07-28-1998	Schaefer et al.	
6.	6,023,566		02-08-2000	Balkhale et al.	
7.	6,301,696	B1	11-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date (year(s)), volume/issue number(s), publisher, city and/or country where published.
	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.
	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.

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				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et.al.
				Group Art Unit	2825
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		Number	Kind Code ² (if known)		
1.	5,311,442			Fukushima	
2.	5,526,276			Cox et al	
3.	5,752,000			McGeer et al	
4.	6,086,626			Jain et al	
5.	6,102,964			Tse et al	
6.	6,134,705			Pedersen et al	
7.	2001/013113			Matsunaga	
8.	6,298,472			Phillips et al	
9.	6,336,208			Mohan et al	
10.	6,473,884			Ganai et al	
11.	6,490,717			Pedersen et al	
12.	6,546,539			Lu et al	

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Serial/Patent No.: 10/061,459

Filing Date: 1/31/02

Atty Docket: SPLX.P0091

Applicant(s): Steven Teig, et.al.

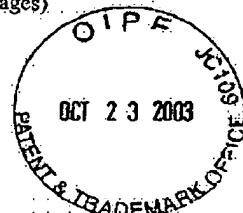
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TITLE: Method and Apparatus for Producing a Circuit Description of a Design

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2. Information Disclosure Statement (2 pages)
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4. (12) cited references



Serial/Patent No.: 10/061,459

Atty/Secty: MA/es

Filing Date: 1/31/02

Atty/Secty: MA/es

Serial/Patent No.: 10/061,459

Date Mailed: 12/1/2003

Filing Date: 1/31/02

Atty Docket: SPLX_P0091

Applicant(s): Steven Teig, et al.

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Serial/Patent No.: 10/061,459
Filing Date: 1/31/02
Atty Docket: SPLX P0091
Applicant(s): Steven Teig, et.al.

Atty/Secty: GS/ES
Date Mailed: 4/6/2004

TITLE: Method and Apparatus for Producing a Circuit Description of a Design

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Serial/Patent No.: 10/061,459
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Atty/Secty: GS/ES
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